



A CMOS Power Amplifier using Back-off Efficiency Enhancement Technique

Seungwon Park and Sanggeun Jeon

School of Electrical Engineering, Korea University, Seoul 136-713, Korea

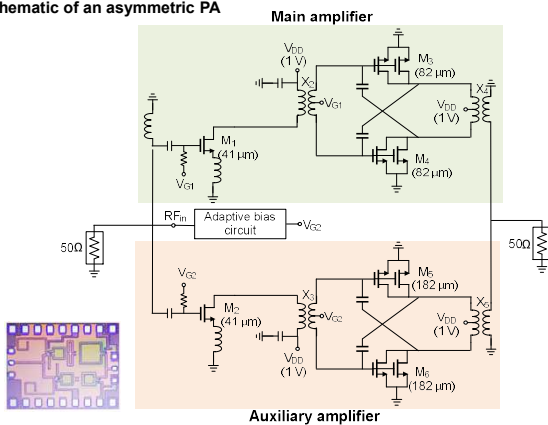
Introduction

- Power amplifier (PA) is one of the most challenging RF blocks in CMOS technology
 - Due to low breakdown voltage and high substrate loss
- Several CMOS mm-wave PAs have been reported as the gate length scales down [1]-[2]
- Especially, a back-off PA is actively reported to support advanced modulation technique

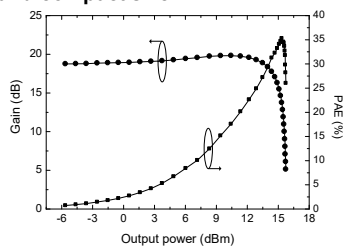
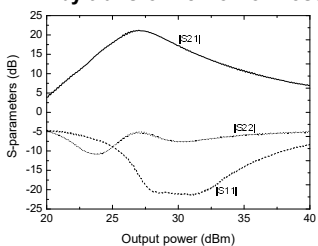


Design

- Schematic of an asymmetric PA

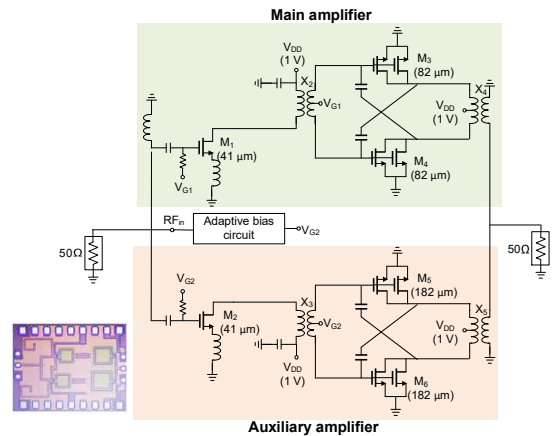


- 2-stage current combined power amplifier
- Each transistor cell is composed of two unit transistors combined for high operating frequency and output power
- For high back-off efficiency, implemented power amplifier is composed by auxiliary and main amplifiers
- Output stages of each amplifier have different transistor gate width to achieve high back-off efficiency
- To further increase back-off efficiency, adaptive bias network (ABN) is adopted and the DC output of ABN is connected to gate bias of the auxiliary amplifier
- The inter-stage and output matching network are implemented by transformer for low loss and compact size

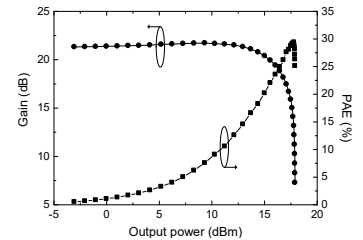
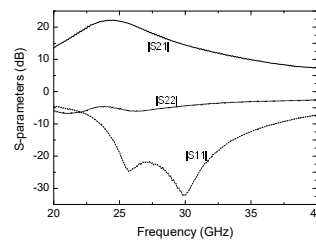


- In measurement, the PA exhibit a peak gain of 21.2 dB at 27 GHz
- The saturation output power and peak PAE are measured at 15.7 and 14.3 dBm at 30 GHz
- The measured peak PAE and 6-dB back-off PAE are 35.3 % and 15.2 %, respectively.

- Schematic of an asymmetric PA with cascode



- To achieve higher back-off efficiency, cascode amplifier is adopted in power stage of auxiliary amplifier
- Furthermore, due to the cascode amplifier, higher output power is expected



- In measurement, the PA exhibit a peak gain of 22.2 dB at 24.5 GHz
- The 3-dB bandwidth is 5.6 GHz from 21.8 to 27.4 GHz
- The saturation output power and peak PAE are measured at 17.9 and 15 dBm at 30 GHz
- The measured peak PAE and 6-dB back-off PAE are 29.4 % and 12.6 %, respectively.

Conclusion

- Back-off efficiency enhanced CMOS PAs are fabricated in a 28-nm CMOS technology
- A proposed asymmetric PA (ver1) shows peak gain of 21.2 dB at 27 GHz and 3-dB bandwidth of 4.3 GHz.
- The measured saturation output power and peak PAE are 15.7 dBm and 35.3 %.
- A proposed another asymmetric PA (ver2) shows saturation output power of 17.9 dBm and peak PAE of 29.4 %.
- The back-off efficiency is improved by adaptive bias network and asymmetric design

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